UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/677,120	09/29/2000	Keith Glidewell	40921/205584	2023

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EXAMINER
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ART UNIT	PAPER NUMBER
2127	

DATE MAILED: 10/04/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

	Application No.	Applicant(s)
Office Action Summary	09/677,120	GLIDEWELL, KEITH
	Examiner	Art Unit	
	Nilesh Shah	2127	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE _3_ MONTH(S) FROM
THE MAILING DATE OF THIS COMMUNICATION.
- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed
  after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
  Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any
  earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on _23 June 2004_.

2a) ☒ This action is **FINAL**.   2b) ☐ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is
closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) _1-6 and 9-21_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) _1-6,9-21_ is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage
application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)

2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4) ☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5) ☐ Notice of Informal Patent Application (PTO-152)

6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-6,9-21 are presented for examination.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as
> set forth in section 102 of this title, if the differences between the subject matter sought to be
> patented and the prior art are such that the subject matter as a whole would have been obvious
> at the time the invention was made to a person having ordinary skill in the art to which said
> subject matter pertains. Patentability shall not be negatived by the manner in which the
> invention was made.

3. Claims 1-6,9-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Alfieri (5,745,778) in view of Kimmel et al (6,105,053) (hereinafter Kimmel)

4. Alfieri was cited by applicant in IDS filed on 10/21/01

5. As per claim 1 Alfieri teaches the invention substantially as claimed including a

method of allocating resources in a plurality of processors system each processor

of said plurality having a cache associated therewith (fig. 1 element 100-108, col.

1 lines 33-36, col. 2 line 43), comprising:

when at least one processor of said plurality of processors system is idle, detecting

at least one other processor of said plurality of processors is not idle (col. 8, lines

62-67).

6. Alfieri does not specifically teach the use of a predetermined period of time

during which as least one processor remains not idle.

Kimmel teaches a method timing a predetermined period of time during which

said at least one other processor which is not idle remains not idle and poaching a

process when the predetermined period of time has elapsed (col. 14 lines 37-45);

and poaching a process on a queue of the at least one non-idle processor to be run

by said at least one processor which is idle (col. 10 – line 60-col. 11 line 5, col. 12

line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

7. It would have been obvious to one skilled in the art at the time of the invention to

combine the teachings of Alfieri and Kimmel because Kimmel's timing would

maximize the throughput of the Alfieri's system by poaching a task from a non-

idle processor to an idle processor only when the predetermined period of time

has elapsed.

8. As per claim 2, Kimmel teaches a method wherein if more than one processor is

idle, poaching the process with the idle processor which is electrically closest to

the at least one non-idle processor (col. 10 – line 60-col. 11 line 5, col. 12 line 12-

15, col. 14 lines 11-12 and col. 14 lines 37-45).

9. As per claim 3, Kimmel teaches a method wherein the time period during which a non-idle processor is allowed to remain non-idle is greater the farther away a non-idle processor is electrically located relative to an idle processor. (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

10. As per claim 4, Kimmel teaches a method wherein an idle processor will first try to poach from a non-idle processor electrically closest to it, and if the processor electrically closest to the idle processor is idle, it will then try to poach from the next processor which is electrically closest to it until it encounters a non-idle processor on which poaching can occur (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

11. As per claim 5 Kimmel teaches a ccNUMA system (col. 4 lines 17-30).

12. As per claim 6, Kimmel teaches a method wherein each processor starts a timer associated therewith when it goes non-idle, and allowing an idle processor to poach a process therefrom only when a predetermined amount of time has elapsed on the timer (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

13. As per claim 9, is rejected for the same reason as claim 2 above. Alfieri did not specifically teach a method wherein said processor system is a four block system.

However, Alfieri disclosed a multiprocessor system (Fig. 1) that could include a

plurality of processors. It would have been obvious to one skilled in the art to

have included 16 processors in Alfieri's system.

14. As per claim 10, Kimmel teaches a method wherein in the event more than one

idle processors attempt to poach a process from a non-idle processor, allowing the

idle processor in closest electrical proximity to the non-idle processor poach the

process (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and

col. 14 lines 37-45).

15. As per claim 11 Alfieri teaches a data processing system for allocating resources

for simultaneously executing a plurality of processing tasks, comprising:

a plurality of processors, each having a cache associated therewith (fig. 1 element

100-108, col. 1 lines 33-36, col. 2 line 43)

means for detecting at least one other processor of said plurality of processors

which is not idle and for determining the duration of time any one of said at least

one other processor is not idle(col. 8 lines 62-67).

Kimmel teaches a timer associated with each processor for timing from the

beginning of receiving a process from the processor's queue, the duration of time

the process is rum, during which time the processor is running the process is non-

idle (col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45, col. 10 – line

60-col. 11 line 5);

means for then poaching a process from a non-idle processor by an idle processor

when said duration of time during which the non-idle processor is running a

process exceeds a predetermined amount (col. 10 – line 60-col. 11 line 5, col. 12

line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

16. Claims 12-16 are rejected based on the same rejections as claims 2-6 above.

17. As per claim 17, Kimmel teaches a system wherein said predetermined amount of

time is established in relation to electrical proximity between an idle processor

and a non-idle processor (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col.

14 lines 11-12 and col. 14 lines 37-45).

18. As per claim 18, Kimmel teaches a system wherein the greater the electrical

distance between idle and non-idle processors, the greater the predetermined

amount of time which is allowed to elapse for said non-idle processor (col. 10 –

line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-

45).

19. Claim 19 is rejected based on the same rejection as claim 9 above.

20. As per claim 20, Kimmel teaches a system wherein said processors are configured

for allowing an idle processor in closest electrically closest to a non-idle processor

to poach a process therefrom in the event more than one idle processor attempts to

poach a process from said non-idle processor (col. 10 – line 60-col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

21. As per claim 21 Alfieri teaches a method of allocating resources in a plurality of processors system, each processor of said plurality having a cache associated therewith, comprising (fig. 1 element 100-108, col. 1 lines 33-36, col. 2 line 43): when at least one processor of said plurality of processors of said system is idle detecting at least one other processor of said plurality of processors which is not idle (col. 8, lines 62-67);

Kimmel teaches if said at least one other processor which is not idle remains not idle when the predetermined period of time has elapsed on the timer then poaching a process therefrom with an idle processor (col. 14 lines 37-45); and starting a timer at said at least one other processor when it goes not idle, and timing a predetermined period of time during which said at least one other processor which is not idle remains not idle (col. 8, lines 62-67, col. 14 lines 37-45);

conducting said poaching in a manner which an idle processor first ties to poach from a non-idle processor electrically closest to it, and if the processor electrically closest to the idle processor is idle, trying to poach from the next processor which is electrically closest to it until it encounters a non-idle processor on which poaching can occur and wherein tile predetermine time period during which a non-idle processor is allowed to remain non-idle is greater the farther electrically

away a non-idle processor is located relative to an idle processor(col. 10 – line 60-

col. 11 line 5, col. 12 line 12-15, col. 14 lines 11-12 and col. 14 lines 37-45).

Response to Arguments

21. Applicant's arguments filed 6/23/04 have been fully considered but they are not

persuasive.

In the remark applicant argued: (a) Kimmel fails to teach after a predetermined

period of time has elapsed THEN the process of poaching occurs.

Examiner respectfully disagrees with applicants argument: As per (a), Kimmel

clearly teaches the use poaching after a predetermined time has elapsed (col. 14

lines 37-45). After the predetermined time then poaching can occur (fig. 4b

elements 661,621).

Conclusion

22. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of

time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire

THREE MONTHS from the mailing date of this action. In the event a first reply

is filed within TWO MONTHS of the mailing date of this final action and the

advisory action is not mailed until after the end of the THREE-MONTH

shortened statutory period, then the shortened statutory period will expire on the

date the advisory action is mailed, and any extension fee pursuant to 37

CFR 1.136(a) will be calculated from the mailing date of the advisory action. In

no event, however, will the statutory period for reply expire later than SIX
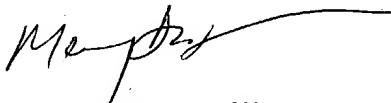
MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications

from the examiner should be directed to Nilesh Shah whose telephone number is

(571)272-3771. The examiner can normally be reached on 9-5.

If attempts to reach the examiner by telephone are unsuccessful, the

examiner's supervisor, Meng An can be reached on (571)272-3756.

Information regarding the status of an application may be obtained from

the Patent Application Information Retrieval (PAIR) system. Status information

for published applications may be obtained from either Private PAIR or Public

PAIR. Status information for unpublished applications is available through

Private PAIR only. For more information about the PAIR system, see http://pair-

direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nilesh Shah
Examiner
Art Unit 2127

NS
September 28, 2004

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